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Support / Wiki:

Silicon Radar GmbH
Im Technologiepark 1
15236 Frankfurt (Oder)
Germany

fon +49 (0) 335 228 80 30
fax +49 (0) 335 557 10 50
https://www.siliconradar.com
https://wiki.siliconradar.com

SiRad MIMO r2
System Description

User Guide

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1.0	all		Initial document

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1 General Conception

The platform consists of two stacked boards, a universal baseband board and an interchangeable Radar Front End (RFE) board with a radar transceiver chip. The baseboard performs radar signals digitalization, processing and transferring to a host computer (PC). Changing the RFE board allows the use of radar configurations with different frequency bands, antenna configurations, etc.

The baseband board is pictured in Figure 1 with the connectors and microcontrollers labelled.

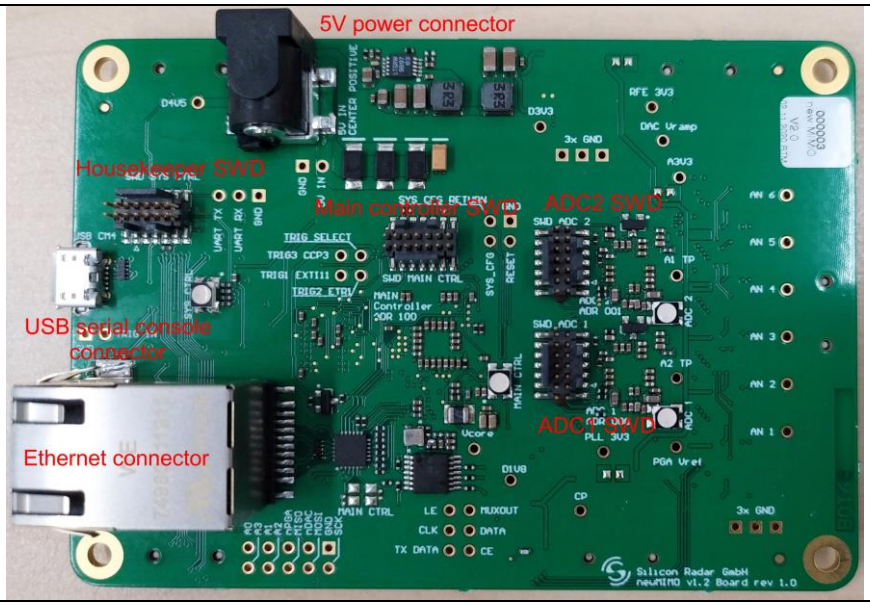

Figure 1: Baseband board

As an example, the 24GHz RFE board is shown in Figure 2.

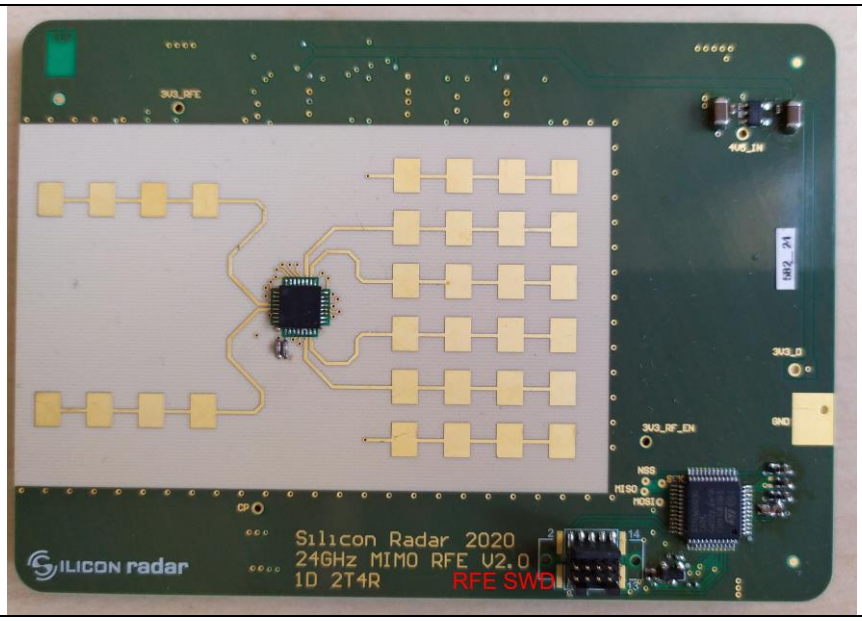

Figure 2: 24GHz RFE board

1.1 The baseboard design

The functional block diagram of the baseboard is depicted in Figure 3.

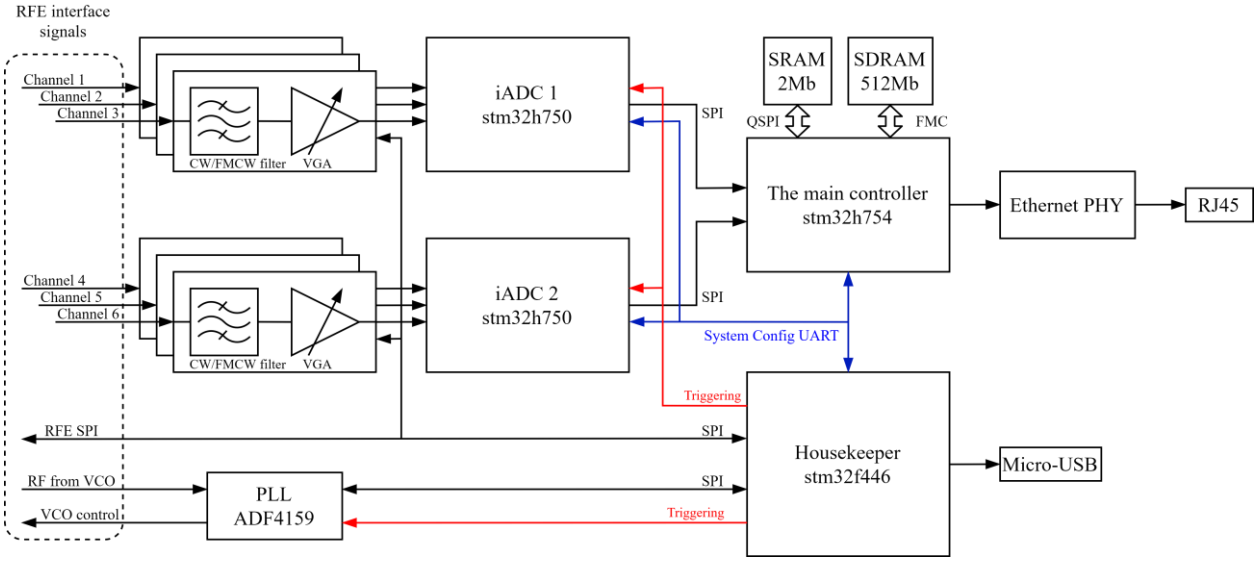

Figure 3: Baseband board functional block diagram

The baseband radar signals from the chip are filtered and amplified (with user selectable variable gain), before being sampled by two microcontrollers named iADCs (intelligent analog to digital converter). Each iADC digitizes three receive channels with a maximum sampling frequency of 2.5MHz. The iADCs capture a number of ramps from active transmit channels and thus form a “data cube” in memory. A data cube can be considered a group of digitized ramps collected from all activated transmit and receive channels on which all first level (DC cancellation, windowing, 1-D Fourier transform, target detection etc.) and second level processing (Doppler estimation, angular estimation) takes place. It can also be viewed as the unit of data required to generate a frame in the GUI.

The iADC can be configured to output data at various points along the processing chain, for instance raw ADC sample data, FFT output data etc. Once ready, data is transferred to the main controller.

The main controller may perform second stage processing like various Direction of Arrival (DOA) algorithms, Doppler-Range estimation, etc. but the primary role of the main controller is sending data to a host PC for visualization and analysis. Data transmission is performed over the Ethernet interface by the UDP protocol.

A further microcontroller controls all parts of the system, generates sampling and ramp sequences, provides command interface for system configuration and control. It is called the Housekeeper. The command interface with the Housekeeper is text-based and implemented via the USB-Serial interface.

The Housekeeper also interacts with the RFE board via the SPI interface to detect its type, to switch transmission antenna and to perform some configuration.

The baseband board also integrates a PLL chip. It gets a divided RF carrier signal form the radar chip and forms a control signal to sweep (or set statically) frequencies according to the ramp sequence.

1.2 The RFE design

SiRad MIMO r2 RFE_T2R4_024_020

The SiRad MIMO r2 RFE_T2R4_024_020 board has two transmit and four receive antennas. The radar transceiver chip is controlled via SPI interface. The board has dedicated microcontroller to control the transceiver chip and to interact with the baseboard.

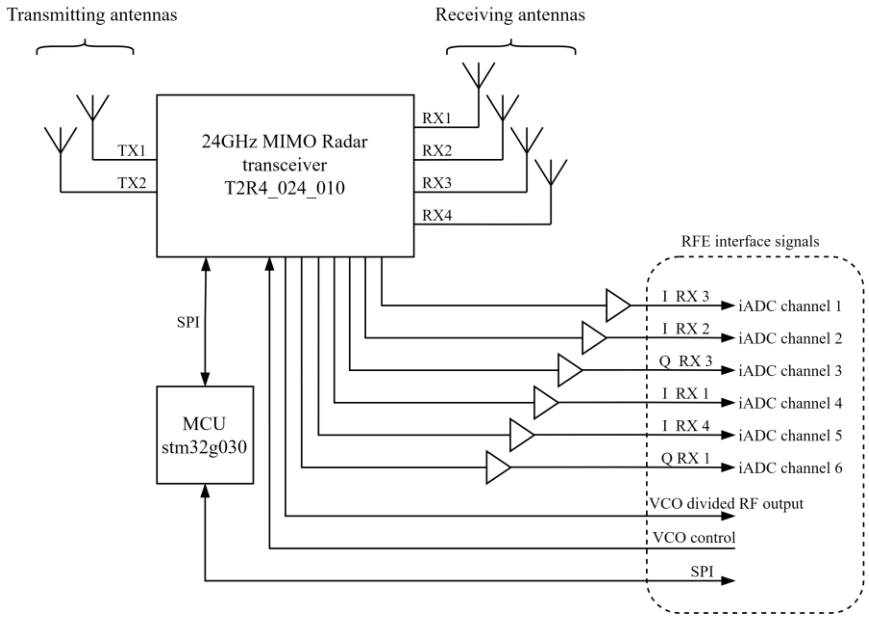

Figure 4: 24GHz RFE functional block diagram

The RFE board provides six analog output signals as depicted in Figure 4. Two RX channel have full set of quadrature components (I and Q) and two channels provide only in-phase (I) components.

The physical antenna placement and numbering is depicted in Figure 5. Additional antennas are included on the Rx array to provide electromagnetic symmetry.

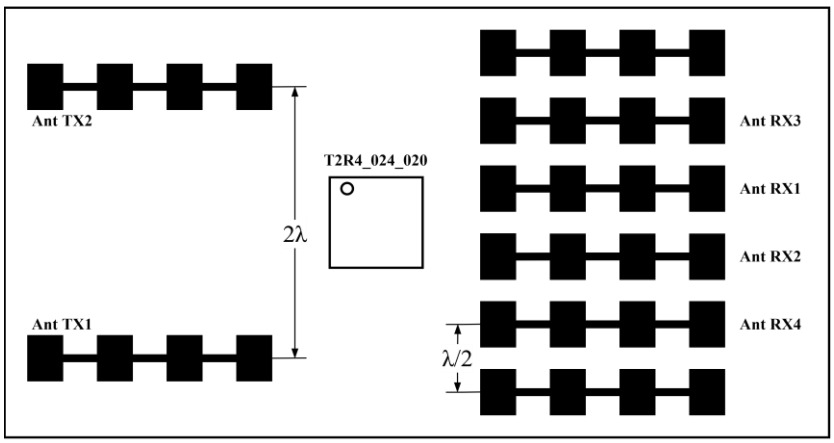

Figure 5: 24GHz RFE patch antenna

2 Triggering Description

The sample triggering process is controlled by the Housekeeper controller which generates iADC sampling pulses and starts PLL sweeps according to a ramp structure. Internally the triggering process is based on a 10 MHz clock. All time intervals are taken as number of the 10 MHz clock pulses.

In the Figure 8 a simplified timing diagram of triggering process is displayed.

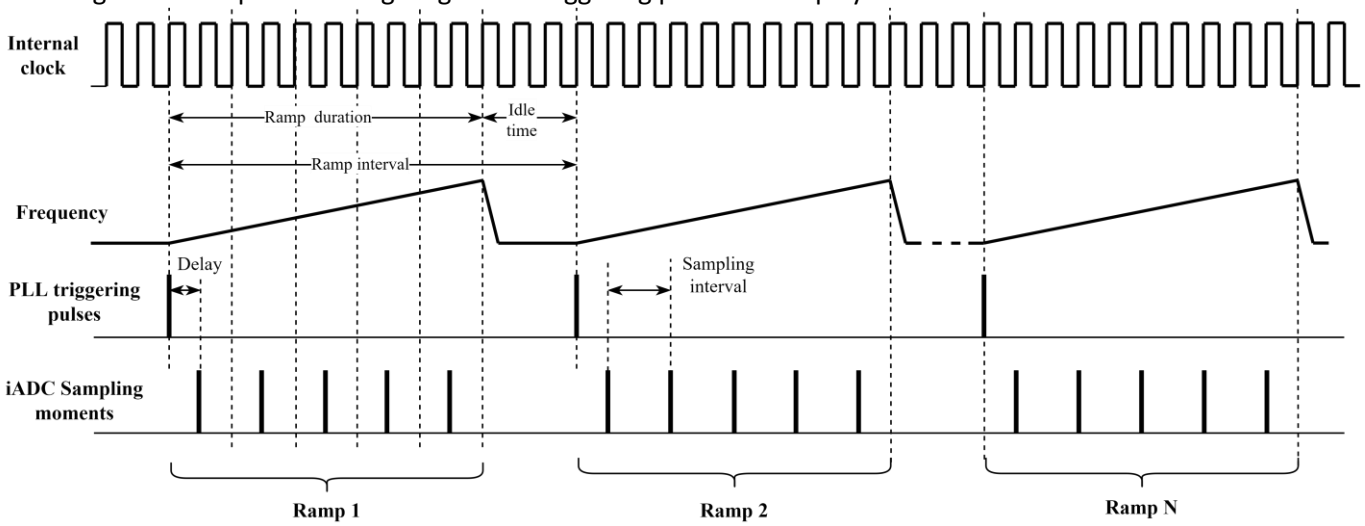

Figure 6: Sample triggering process

The idle interval is intended to restore the PLL frequency to an initial value. The same time the Housekeeper communicates with the RFE boards and sends command to switch the TX antenna. This take about 50us. Therefore the idle time should not be setup less than this value.

The triggering is configured by the *trg* command and has four parameters (further documented in Chapter 3).

The first parameter defines the sampling interval. Its minimum value is si = 4 which gives 4/10MHz = 0.4us sampling interval or 2.5Mhz sampling frequency.

The second parameters is the number of samples per ramp which defines the ramp duration. For example, sc=512 sampling pulses corresponds 512 * 0.4us = 204.8us ramp duration in case of si = 4.

The third parameters ri defines the ramp interval which the user has to take care of himself and which should be chosen to be at least 50us greater than ramp duration. For example, if si = 4 and sc = 512, ri may be chosen equal to 3000 that gives the ramp interval 3000/10MHz = 300us and the idle time about 300us – 204.8us = 95.2us.

And the last parameter rc is number of ramps in a data cube. Its value should be power of two and has minimum value 32.

For each ADC channel there is a buffers of 65536 samples length. So it is possible to have various combinations of number of ramps and sampling pulses per ramp to keep data in the buffer. For example, it is possible to setup 128 ramps x 512 samples, or 64 ramps x 1024 samples and so on.

The data cube of sc samples and rc ramps is collected inside iADC and the transferred to the main controlled which sends data to the host PC. Then this process may be manually or automatically repeated by *trg:start* command (Chapter 3).

3 The Baseboard Command Interface

The command interface operates via USB interface. Connection the board to a Windows-based host PC creates a virtual serial port. It supports 115200bps 8-N-1 mode. A terminal program has to be setup to transmit CR+LF at the end of a line.

The set of commands is presented in the table below.

Table 1: Command list

Command	Function	Notes	Example
trg:si;sc;ri;rc	Setup triggering parameters	**si** - sampling interval, minimum value 4 **sc** - sample count, must be power of two, the minimum value 32, maximum 2048 **ri** - ramp interval, must be greater than **si * sc** **rc** - ramp count, must be power of two, the minimum value 32	*trg:4;512;3000;32*
trg:start[;r;n]	Start trigger sequence	Optional parameters to setup triggering repetition r – repetition period in ms n – number of repetition, parameter may be skipped for indefinite repetition	*trg:start* *trg:start;50*
trg:stop	Stop trigger sequence		trg:stop
pga:x;x;x;x;x;y	Setup PGA gains and filtering	Gain values x must be in the range 0..8 0 - PGA off 1 - +0 2 - +6 3 - +12 4 - +14 5 - +18 6 - +20 7 - +24 8 - +30 Filtering: 0 – for CW mode; 1 – for FMCW mode	*pga:2;2;2;2;2;2;1*
ips:x.x.x.x	Setup board's IP address		*ips:192.168.0.5*
ipd:x.x.x.x;p	Setup host's IP address, port		*ipd:192.168.0.1;5001* Port must be in the range 1023…65535
freq:x	Setup start frequency for	x – Frequency value in Hz.	*freq:25000000000*

	the ramping process		
bw:x	Setup bandwidth for the ramping process	x – Bandwidth value in Hz.	*bw:3000000000*
rfei	Get RFE configuration	This request returns frequency band, number of TX antennas, number of RX antennas	

Recommended command sequence:

1. Set up PGA/baseband gains.
2. Set up triggering parameters.
3. Start trigger.
4. Stop trigger (if triggering with repetition interval).

4 Data Interface

Data transmission is performed via Ethernet using UDP. The current implementation uses static IP configuration. By default the base board has IP address 192.168.0.1 and it sends UDP data stream to the address 192.168.0.1, port 5001. Both addresses may be changed via command interface. But the baseboard keeps setting till reset or power down/up cycle.

The network stack supports ping functionality which may be used for diagnostics.

In case of using the kit with Windows OS, attention should be paid to the firewall settings. For example native Windows firewall drops incoming UDP packets by default.

The data stream has the following format:

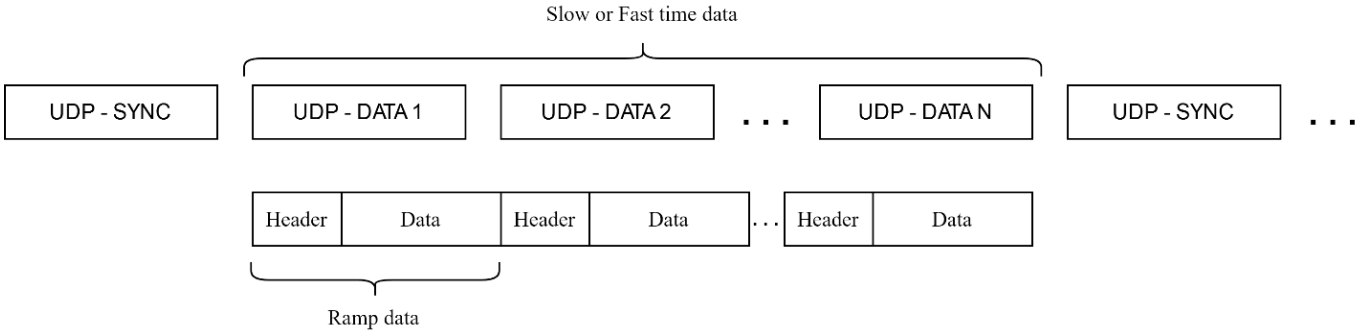

Figure 7: Data stream format

The stream consist of periodic SYNC and DATA packets. The SYNC packets are intended to setup a synchronization among the stream and transmitted by one UDP packet. Data is transmitted by the necessary number of UDP packets.

The data portion consists of ramp data fields. Each of them has a header and a data payload.

The SYNC packet consists of 24 bytes and may be described by the following structure:

```
typedef struct
{
        uint32_t syncWord_1;
        uint32_t syncWord_2;
        uint64_t frameCnt;
        uint32_t dataLen;
        uint32_t crc;
} SyncFrame_t;
```

where syncWord_1 = 0x12345678, syncWord_2 = 0xAA55AA55, frameCnt is a counter which is increased every SYNC packet, dataLen is amount of data bytes following SYNC, crc is an optional CRC-32.

The format of the data portion is as follows in Figure 10.

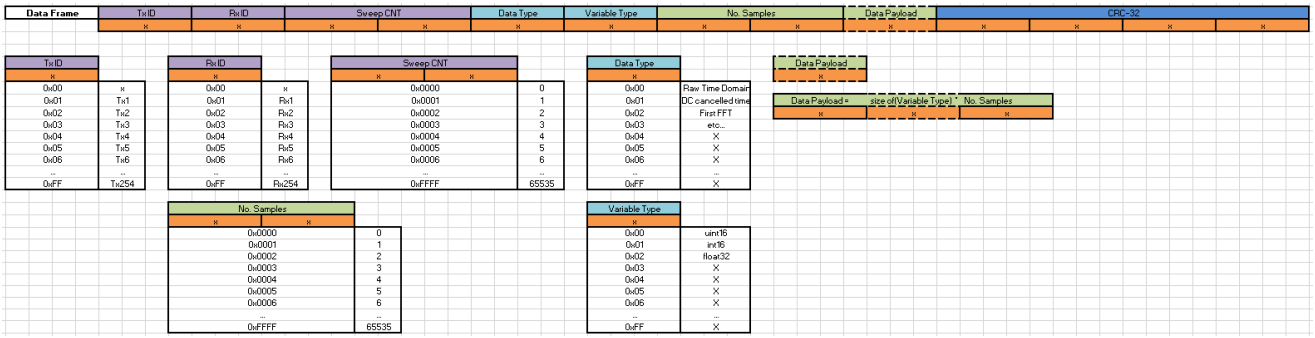

Figure 8: Data frame format

The TxID and RxID field are used to label the transmit and receive channel (thus virtual channel) from which the data in the payload relates to.

The Sweep CNT gives the ramp number of a particular virtual channel. I.e. the first ramp from transmitter Tx1 to receiver Rx1 will have a Sweep CNT of 1, the second will ramp from transmitter Tx1 to receiver Rx1 will have a Sweep CNT of 2 etc..

The Data Type field details the form of the data in the payload. In essence it defines the preprocessing steps that have taken place on the data. As features are added to the firmware, further options will be added to the Data Type field.

The variable type field gives the format of each sample point in the payload. For example, Raw Time Domain data comes in the form of unsigned 16-bit integer ADC values, whereas FFT points are 32-bit floating point values.

The No. Samples field gives the number of sample points in the payload.

In order to determine the total size of the Data Payload in bytes, the Variable Type and No. Samples field must be examined together. For example; 512 Raw Time Domain data points will give a data payload of 2 × 512 = 1024 bytes, whereas 512 FFT points will give a data payload of 4 × 512 = 2048 bytes.

When determining the size of the entire data frame, the size of the header and CRC must be factored in also.

5 Firmware Update Procedure

The platform has five programmable parts with upgradable firmware:

- Housekeeper MCU
- The main controller MCU
- Two iADC MCU
- RFE board MCU

The listed MCUs are manufactured by ST Microelectronics and should be programmed by STLINK-V3MINI debugger and STM32 ST-LINK Utility.

The firmware is provided in the form of binary files with the following naming:

- F446-Housekeeper – housekeeper firmware
- H745-MainController_CM7.bin – the main controller firmware
- H750-iADC.bin - the iADC firmware (identical for both)
- RFE_Controller.bin – RFE controller firmware

The firmware updating is performed using the same steps for each MCU. The only difference is physical SWD connector used. The baseboard has four SWD connector and RFE board has one. Refer to the Figures 1 and 2 for specific locations.

In the Figure 11 an example of ST-LINK cable connection is depicted.

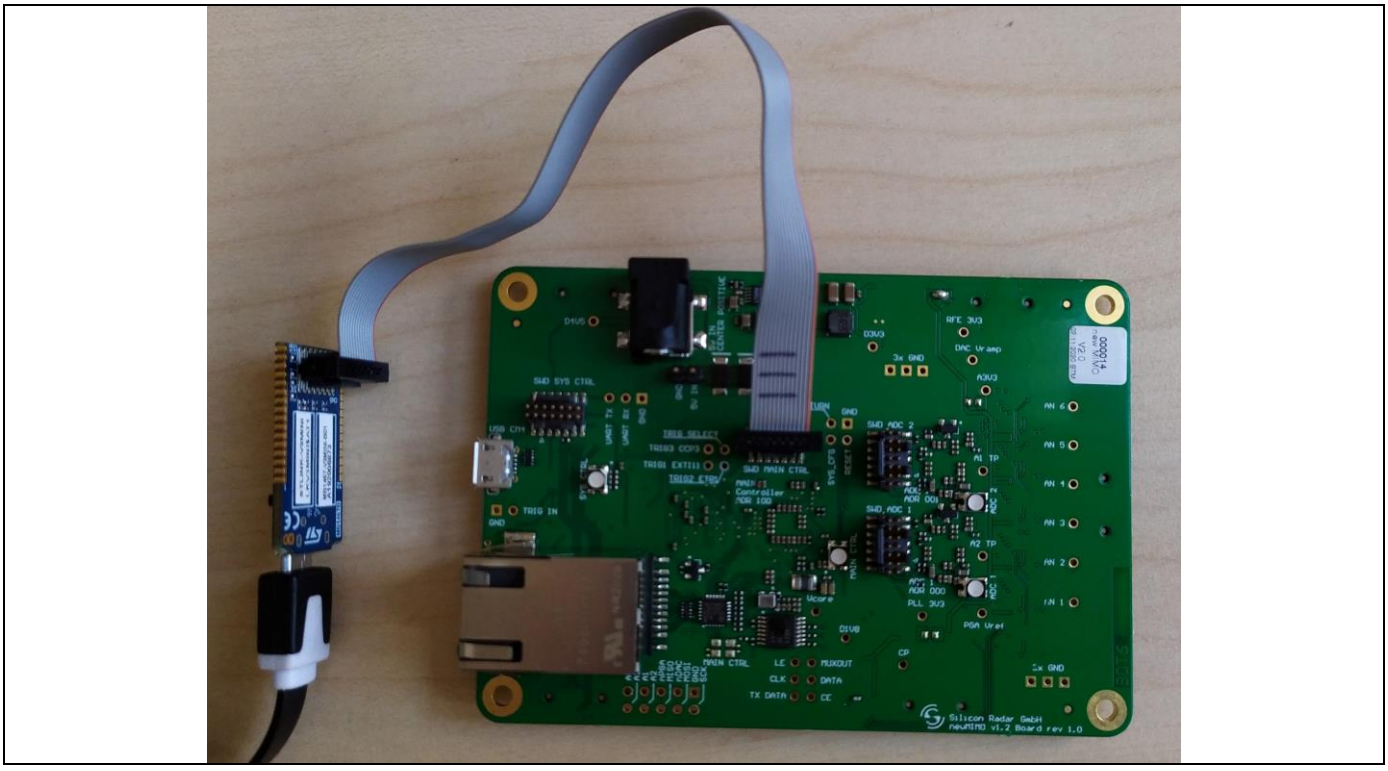

Figure 9: ST-LINK Mini connection to the main controller SWD interface

The firmware upgrade is performed by the following steps:

1. Disconnect power source from the main board.
2. Connect STLINK-V3MINI cable to an appropriate SWD connector.
3. Run STM32 ST-LINK Utility.
4. Power up the baseboard
5. In the STM32 ST-LINK Utility select menu “Target”/”Connect”.

In case of successful connection with a target the program has to report in its status windows. In case of the old STLINK-V3MINI (see Accessories) internal firmware ST-LINK Utility [5] may require to update it.

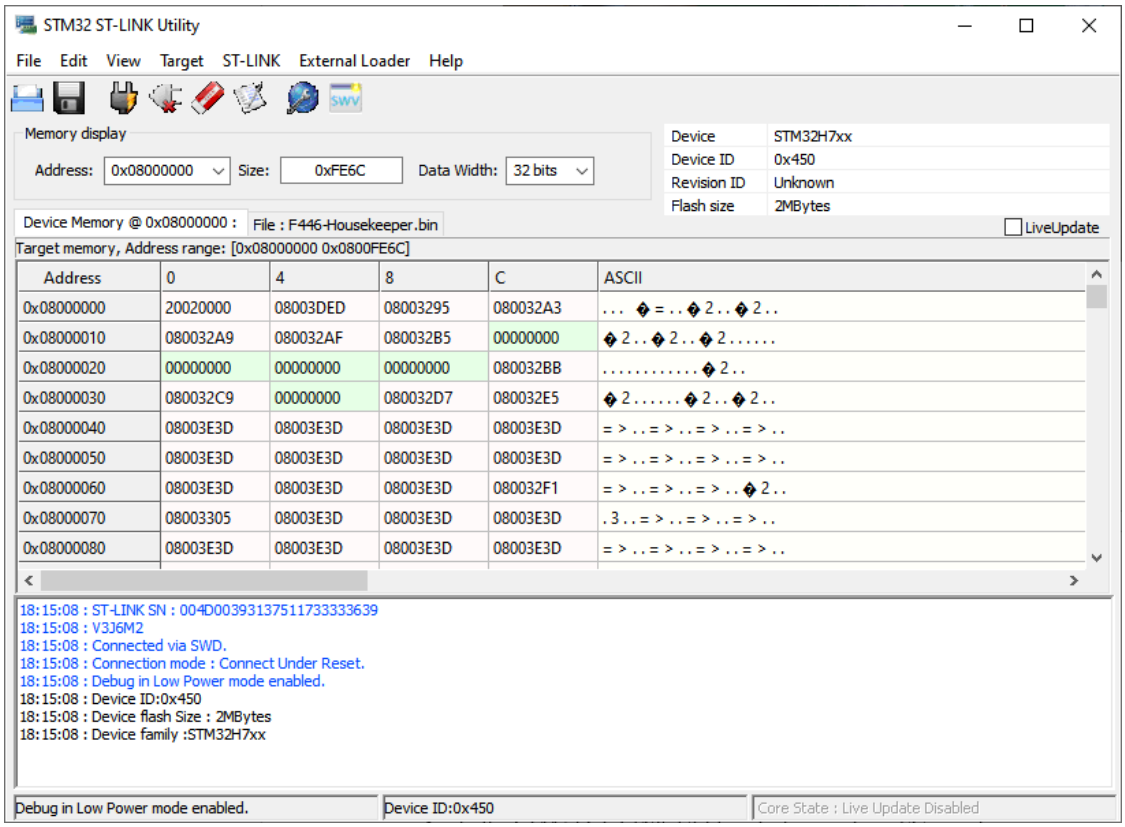

Figure 10: ST-LINK Utility view

6. Open an appropriate binary file by “File”/”Open file” menu.
7. Flash firmware by “Target”/”Program&Verify” menu.
8. Disconnect target by “Target”/”Disconnect”
9. Disconnected power source from the main board.
10. Detach STLINK cable.

6 Accessories

Baseband Board	Order Nr.	Description
USB-MicroB-Cable	3rd party vendor	Standard shielded USB cable type A to micro-B. Available from most distributors of electronic components like Farnell, Digi-Key, or Mouser.
STLINK-V3MINI	3rd party vendor	Debugger / programmer, for example, from Mouser or RS Components, Mfr. No.: STLINK-V3MINI.
Ethernet Cable	3rd party vendor	Standard Shielded Ethernet cable from most distributors of electronic components like Farnell, Digi-Key, or Mouser.

References

[1] https://siliconradar.com/products/
[2] https://login.siliconradar.com/
[3] https://siliconradar.com/wiki/
[4] https://realterm.sourceforge.io
[5] https://www.st.com/en/development-tools/stsw-link004.html

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